DOCUMENT-IDENTIFIER: US 6609167 B1
TITLE: Host and device serial communication protocols and communication packet formats

Detailed Description Text (30):
FIG. 8 shows a more detailed diagram of the ASP Host Controller 104a, which consists of a system bus interface and an ASP bus interface. These two interfaces provide data flow between the host and the ASP devices 106. In one preferred embodiment, the ASP Host Controller 104a can support one outstanding command per device. The system bus interface allows the system software by way of a system bus 164 to communicate with the ASP devices. It provides a mechanism to transfer data to and from the host memory, and a mechanism to send notifications to the system software. In one embodiment, it uses a DMA controller to transfer data to and from the host memory, and uses an interrupt to send a notification to the system software at successful command completion or abort due to errors. In one preferred embodiment, the Host Controller also supports scatter/gather data transfers. The ASP Host Controller 104a supports a mechanism to accept ATA/ATAPI commands. The system bus interface may contain some configurable parameters. Some of these configurable parameters include: (a) capabilities of the host controller; (b) configurable link speeds, packet sizes, and repeat counts per device; (c) globally and individually maskable interrupts, and interrupt status; (d) device attachment information; and (e) mechanisms to start a command execution and data transfer.

Detailed Description Text (34):
In accordance with the present invention, ASP can issue one outstanding command per device to the ASP Host Controller 104a. Thus, all devices can overlap their command executions. The HCD also provides the memory addresses and transfer counts to the ASP Host Controller 106, and the data transfer is performed by the DMA controller. Also, the value at offset 0, which was used for PIO data transfers, is no longer used. The use of DMA commands and the use of LBA addressing instead of CHS addressing are now used. The following data elements contain the relevant information for a request: (a)an ATA command and optionally an ATAPI command, and an ATA status; (b) data transfer information indicating the addressed device, whether data transfer is involved, and the direction of the data transfer; and (c) physical memory addresses and transfer counts of a list of scatter/gather data buffers.

Detailed Description Text (207):
FIG. 42 shows a command execution flow 400 of the present invention which involves the following operations: 1. The CPU 402 sets up a Command Descriptor Block (CDB) 404 with an ATA/ATAPI command and a scatter/gather list in system memory. 2. The CPU 402 writes the address of this CDB to the CDB Pointer Register of the ASP HCI 408. 3. The host controller sets the DMA controller to transfer the CDB to internal memory. 4. The host controller 408 sends the command to the device and sends IN packets to poll the device 106 for data. 5. The device responds with data packets. 6. The host controller sets up the DMA controller to transfer the data to the data buffers 406 pointed to by the scatter/gather list. 7. The host controller 408 sets up the interrupt status and interrupts the CPU 402.

Detailed Description Text (209):

The HCI data structures include a command descriptor, a data transfer descriptor, and a scatter/gather list. The command descriptor consists of an ATA and ATAPI command. The data transfer descriptor specifies the device address, and data transfer direction and count. The scatter/gather list specifies a list of physical memory addresses and transfer counts for data transfers. In a preferred embodiment, the Host Controller data structure should be in one contiguous block of double-word aligned physical memory. The Host Controller is given a pointer to this data structure to start a command execution. The following Tables 44 and 45 illustrate a format of the Host Command Descriptor Block (CDB).

Detailed Description Text (218):
The scatter/gather list specifies the physical memory addresses and sizes of the data buffers in system memory, and may contain any number of entries. The EOT bit indicates the end of this list. However, a maximum of 16 segment entries is recommended. Physical memory addresses can be byte-aligned. The maximum transfer count is 64 K, and the count should be an even number, and zero indicates 64 K. EOT=End of table.

Detailed Description Paragraph Table (44):
TABLE 44 Host Command Descriptor Block for 32-bit Addressing Offset Length Description Type 0 8 ATA Command/ATA Status Command Descriptor 8 16 ATAPI Command 24 4 Data Control Data Transfer 28 4 Total Transfer Count Descriptor 32 4 Segment 0 Physical Memory Scatter/Gather List Address 36 4 Segment 0 Transfer Count 40 4 Segment 1 Physical Memory Address 44 4 Segment 1 Transfer Count . . .

Detailed Description Paragraph Table (45):
TABLE 45 Host Command Descriptor Block for 64-bit Addressing Offset Length Description Type 0 8 ATA Command/ATA Status Command Descriptor 8 16 ATAPI Command 24 4 Data Control Data Transfer 28 4 Total Transfer Count Descriptor 32 8 Segment 0 Physical Memory Scatter/Gather List Address 40 4 Segment 0 Transfer Count 44 8 Segment 1 Physical Memory Address 52 4 Segment 1 Transfer Count . . .

Detailed Description Paragraph Table (52):
TABLE 52 Scatter/Gather Entry for 32-bit Addressing (8 bytes) Byte 3 Byte 2 Byte 1 Byte 0 Physical Memory Address EOT Reserved Transfer Count [15:1] 0

Detailed Description Paragraph Table (53):
TABLE 53 Scatter/Gather Entry for 64-bit Addressing (12 bytes) Byte 3 Byte 2 Byte 1 Byte 0 Physical Memory Address [31:00] Physical Memory Address [63:32] EOT Reserved Transfer Count [15:1] 0